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Results **1** - **20** of about **15,900**. (**0.45** sec)

Virtual memory in contemporary microprocessors — [PDF] from psu.edu
B Jacob ... - Micro, IEEE, 1998 - ieeexplore.ieee.org
... Therefore, required cache or TLB flushing occurs very infrequently, assuming **shared** mem- ory is implemented ... sharing is not desired, the BAT register contents need to be flushed on a **context switch**. ... the table is not guaranteed to hold all active mappings, the **OS** must manage ...
Cited by 60 - Related articles - BL Direct - All 53 versions

[PDF] Aspects of the InfiniBand™ Architecture — [PDF] from uminho.pt
G Pfister - Architecture, 2001 - gec.di.uminho.pt
... assigns LIDs, determines MTUs, loads **switch** routing tables • Provides path information ... to **shared** devices • **Shared** devices have known special semantics: Inter-**OS** locking, etc. Page 18. 18 ... own: – **OS** of A writes on 1A, 2A, 1B, 2B – **OS** of B writes on 1A, 2A, 1B, 2B • Chaos. ...
Cited by 26 - Related articles - All 10 versions

Central **shared** queue based time multiplexed packet **switch** with deadlock avoidance
PH Hochschild... - US Patent 5,546,391, 1996 - Google Patents
... Russell W. Blum Attorney, Agent, or Firm—Floyd A. Gonzalez; James E. Murray [57] ABSTRACT A packet **switch** (25,) contains ... Non-critical chunks are stored within available **shared** slots in the central queue. ... 3 i co- co * => LL co cc L. < . n 1 5C 0 **O O** E •t CO **OS** r— ^*. ^ CO o ...
Cited by 75 - Related articles - All 2 versions

Processor architecture with independent **OS** resources
BK Paracy - US Patent 6,006,320, 1999 - Google Patents
... Since many of the operations that were triggered by the **OS context switch** are no longer necessary, user process consistency is significantly improved. ... In addition, other processing units, such as floating point unit 42 and graphics unit 44 with a **shared** register file 46 are shown. ...
Cited by 7 - Related articles - All 2 versions

Measuring **OS** support for real-time CORBA ORBs — [PDF] from psu.edu
DL Levine, S Flores-Gaitan, CD Gill... - Object-Oriented Real- ..., 1999 - ieeexplore.ieee.org
... **POSIX**. It is de- signed to work on uniprocessors and **shared** memory symmet- ric multiprocessors [24]. ... overhead. Results of **OS context switch** overhead metrics: Table 1 shows the **context switch** times measured on each of the plat- forms. ...
Cited by 19 - Related articles - All 15 versions

Middleware: a model for distributed system services
PA Bernstein - Communications of the ACM, 1996 - portal.acm.org
... For example, a message **switch**, which translates messages between different formats, is considered middleware if it makes it ... Now they are usually bundled with the **OS**. ... it adds value by specializing the user interface, simplifying the API by maintaining **shared context**, or adding ...
Cited by 612 - Related articles - BL Direct - All 5 versions

System for explicitly referencing a register for its current content when performing processor **context switch**
RW Yoder, L McCulley... - US Patent 6,199,156, 2001 - Google Patents
... In a modern operating system (**OS**), there are well-defined tasks that must be accomplished ... is especially important in high volume transaction environments where it is necessary to **switch** back and ... The cache memory system 94 is **shared** among the pro- cessors 92 on the CPU ...
Cited by 15 - Related articles - All 2 versions

MINT: a front end for efficient simulation of **shared**-memory multiprocessors — [PDF] from psu.edu
JE Veenstra ... - Modeling, Analysis, and Simulation ..., 1994 - ieeexplore.ieee.org
... Unlike the cases of a **switch** statement, functions can be separately compiled. ... "**Shared** refs" is the number of references to **shared** memory. ... as integer matrix multiply with high instruction-to-memory-reference ratios -can be simu- lated faster than programs with lo@**os** since there ...
Cited by 373 - Related articles - All 13 versions

Design and performance of Multinet **switch**: A multistage ATM **switch** architecture with partially **shared** buffers — [PDF] from psu.edu
HS Kim - IEEE/ACM Transactions on Networking (TON), 1994 - portal.acm.org
... Wang and Tobagi [19] apply this "divide and conquer" architecture in the **context** of ATM switching for the design of an output queueing **switch**. ... In tlus paper, we present a compromise solution to both dedicated and **shared** queueing **switch** architectures. ...
Cited by 30 - Related articles - All 6 versions

CpG oligodeoxynucleotides act as adjuvants that **switch** on T helper 1 (Th1) immunity — [HTML] from rupress.org
RS Chu, OS Targoni, AM Krieg... - The Journal of ..., 1997 - jem.rupress.org
... These sequences **shared** a CpG motif, containing a central unmethylated CpG dinucleotide preferentially flanked by two 5 ... Thus, the addition of CpG ODN induced a **switch** from a Th2-dominated response to a ... be due in part to the presence of TG dimers in a **context** that provides ...
Cited by 784 - Related articles - BL Direct - All 8 versions

[PDF] Evaluation of rapid **context** switching on a CSRC device — [PDF] from psu.edu
DI Lehn, K Puttegowda, JH Park ... - Proceedings of the ..., 2002 - Citeseer
... Dur- ing **context switch**, the CSLC value is stored in public register if it is to be **shared**, else kept in a ... This layer is based on specific features of the FPGA configura- tion as well as the low level

API features implemented in the basic Operating System (**OS**) running on the ...
Cited by 104 - Related articles - View as HTML - All 2 versions

Implementing priority inheritance semaphore on uC/**OS** real-time kernel
JH Lee ... - 2003 - embedded.org
... If the task has blocked or finished before its quantum has elapsed, the **context switch** is done. ... In case of the uC/**OS** kernel, priority inversion is reduced by priority protection protocol. ... First, it requires static analysis of the system to find the priority ceiling of each **shared** resource. ...
Cited by 3 - Related articles - All 4 versions

Central **shared** queue based time multiplexed packet **switch** with deadlock avoidance
PH Hochschild, ... - US Patent 5,905,889, 1999 - Google Patents
... Specifically, each packet **switch** (25a) contains input port circuits (310) and output port circuits (380) inter-connected ... a message portion ("chunk") destined for only that output port with the remaining slots being **shared** for all ... 0=t- **OS** nJ •× o i f fe 1 3f t C» C z* = c -> LLJ , Li_ or: SL ...
Cited by 33 - Related articles - All 2 versions

Method to suspend-and-resume across various operational environment **contexts**
VJ Zimmer, MA Rothman, MS Doran, ... - US Patent App. 10/ ..., 2003 - Google Patents
... prior to being awakened (block 123), eg, sleep mode is used as a method to **switch** OSs, not ... **skilled** in the art that there could be a X86 Solaris partition, or any other **OS** partition, in ... also be an EFI system partition; in one embodiment, this may be the only **shared** resource partition ...
Cited by 6 - Related articles - All 3 versions

[CITATION] MU C/**OS**: the real-time kernel
JJ Labrosse - 1992 - R&D Publications
Cited by 57 - Related articles - Library Search

OPTS: increasing branch prediction accuracy under **context switch** [PDF] from cisc.edu
MS Lee, YJ Kang, JW Lee, ... - Microprocessors and ..., 2003 - Elsevier
... into several small ones which are **shared** exclusively for each process. Each partition is saved and restored in the main memory like general purpose registers so that **context switch** effects on branch prediction can be mitigated. With the help of the **OS's** scheduling policy, an ...
Related articles - All 19 versions

Adaptive two-level thread Management for fast MPI execution on **shared** memory machines [PDF] from psu.edu
K Shen, H Tang, ... - Proceedings of the 1999 ACM/IEEE ..., 1999 - portal.acm.org
... This paper addresses performance portability of MPI code on multiprogrammed **shared** memory machines. Conventional MPI implementations map each MPI node to an **OS** process, which ... However, kernel threads have **context switch** cost higher than user-level threads and this ...
Cited by 13 - Related articles - All 17 versions

System and method for managing variable weight thread **contexts** in a multithreaded computer system
RP Mank-undaiam - US Patent 5,799,188, 1998 - Google Patents
... of: creating a thread based on resources to which it has access are **shared** with other ... thread state memory area; detecting a thread **context switch**; Operating systems that implement a multithreaded ... the current thread state and restoring a new include the IBM **OS**/2® operating ...
Cited by 28 - Related articles - All 2 versions

Implementation of fast address-space switching and TLB sharing on the StrongARM processor [PDF] from psu.edu
A Wiggins, H Tuch, V Uhlig, ... - Advances in Computer Systems ..., 2003 - Springer
... We also implemented sharing of TLB entries for **shared** pages, a natural extension of the fast-**context**-**switch** approach. ... 1 Introduction A **context switch** occurs in a multi-tasking operating system (**OS**) whenever exe- cution switches between different processes (ie threads ...
Cited by 13 - Related articles - BL Direct - All 32 versions

Shared memory implementation of a parallel **switch**-level circuit simulator
Y Chen, ... - ACM SIGSIM Simulation Digest, 1998 - portal.acm.org
... IRSIM, an ext.entiecl vc,rsion of RSIM, is an event-driven, **switch**- level simulator and ... reported in the following sec- tions were mcasurett from execution on a SPARCIOOO **shared** memory ulachine. The **OS** is Solaris 2.5.1 and it is equipped with 8 SuperSPARC CPUs running at ...
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